WHAT IS CLAIMED IS:

1. A method for patterning layers made of ruthenium or ruthenium(IV) oxide, comprising:

providing a substrate with a substrate surface,

depositing a layer made of ruthenium or ruthenium(IV) oxide on at least sections of the substrate surface;

depositing a covering layer that is inert with respect to oxygen on at least sections of the layer made of ruthenium or ruthenium(IV) oxide, thereby obtaining sections covered by the covering layer and uncovered sections of the layer made of ruthenium or ruthenium(IV) oxide; and

heat treating the substrate in an oxygen-containing atmosphere,

wherein the uncovered sections of the layer made of ruthenium or ruthenium(IV) oxide are converted into a volatile ruthenium oxide and are removed from the substrate surface.

2. The method of claim 1, wherein, during heat treating, the substrate is heated to a temperature of more than 800°C.

3. The method of claim 1, wherein the oxygen-containing atmosphere is formed substantially from oxygen.

4. The method of claim 1, further comprising introducing trenches having trench walls into the substrate and depositing the layer made of ruthenium or ruthenium(IV) oxide on at least sections of the trench walls.

11. The method of claim 1, wherein the covering layer is a layer comprising polysilicon which is passivated with an oxide layer at its surface.

12. A capacitor having a first electrode plate and a second electrode plate and a layer made of a dielectric formed between first electrode plate and second electrode plate, wherein at least one of the electrode plates is formed from ruthenium or ruthenium(IV) oxide in at least sections.

13. The capacitor of claim 12, wherein the capacitor is formed as a trench capacitor in a semiconductor substrate, in which the first electrode plate is formed as a doped section of the semiconductor substrate in a trench wall and the second electrode plate is formed from ruthenium or ruthenium(IV) oxide at least in sections.

14. The capacitor of claim 12, wherein the second electrode plate is formed from at least a layer made of ruthenium or ruthenium(IV) oxide and a layer made of polysilicon.

15. The capacitor of claim 12, wherein the first electrode plate is at least one of supplemented by a layer made of metal and made of an electrically highly conductive material arranged on the doped sections.

16. The capacitor of claim 12, wherein an insulation section is provided in the upper region of the trench wall (7a) adjoining an opening of the trench capacitor.

5. The method of claim 1, further comprising providing a first electrode plate having a high electrical conductivity on the substrate, depositing a layer made of a dielectric on the first electrode plate and depositing the layer made of ruthenium or ruthenium(IV) oxide on the layer made of the dielectric.

6. The method of claim 5, wherein the substrate is a semiconductor substrate and doping of at least sections of the semiconductor substrate results in the first electrode plate being produced as a doped section.

7. The method of claim 6, wherein the first electrode plate is produced by a layer made of metal or a material having a high electrical conductivity being deposited on the doped sections of the semiconductor substrate.

8. The method of claim 5, further comprising depositing a layer made of doped polysilicon on the layer made of ruthenium or ruthenium(IV) oxide.

9. The method of claim 5, further comprising depositing a barrier layer between the first electrode plate and the layer made of a dielectric and/or between the layer made of a dielectric and the layer made of ruthenium or ruthenium(IV) oxide and/or between the layer made of ruthenium or ruthenium(IV) oxide and the layer made of doped polysilicon.

10. The method of claim 1, wherein the heat treating is performed by means of an RTP installation.